

1. (original) A semiconductor circuit comprising:
  - a semiconductor die comprising a first plurality of electrical contacts and a second plurality of electrical contacts;
  - a package substrate comprising a third plurality of electrical contacts and a fourth plurality of electrical contacts;
  - a first plurality of conductive bumps wherein at least one bump in the first plurality serves as at least a portion of a conductive path between at least one of the first plurality of electrical contacts and at least one of the third plurality of electrical contacts;
  - a second plurality of conductive bumps, wherein at least one bump in the second plurality serves as at least a portion of a conductive path between at least one of the second plurality of electrical contacts and at least one of the fourth plurality of electrical contacts; and

wherein each of the bumps in said first plurality of conductive bumps is larger than each of the bumps in said second plurality of conductive bumps.
2. (original) The semiconductor circuit of Claim 1,

wherein the average size of the first plurality of conductive bumps is at least 100% larger than the average size of the second plurality of bumps.
3. (original) The semiconductor circuit of Claim 1,

wherein the average size of the first plurality of conductive bumps is at least 200% larger than the average size of the second plurality of bumps.
4. (original) The semiconductor circuit of Claim 1, wherein the average size of the first plurality of conductive bumps is at least 20% larger than the average size of the second plurality of bumps.
5. (original) The semiconductor circuit of Claim 1, further comprising:
  - a built up layer between the die and the second plurality of bumps; and

wherein the first plurality of bumps are substantially coplanar with the second plurality of bumps relative to the substrate.

6. (original) The semiconductor circuit of Claim 1, further comprising:  
a built up layer between the substrate and the second plurality of bumps; and  
wherein the first plurality of bumps are substantially coplanar with the second plurality of bumps relative to the semiconductor die.
7. (original) The semiconductor circuit of Claim 1, further comprising:  
a first built up layer between the die and the second plurality of bumps;  
a second built up layer between the substrate and the second plurality of bumps;  
and  
wherein the die and substrate are substantially parallel to one another.
8. (original) The semiconductor circuit of Claim 1,  
wherein the substrate comprises a package type selected from the group consisting of a ball grid array, a pin grid array, and a column grid array.
9. (original) The semiconductor circuit of Claim 1,  
wherein the substrate further comprises a plurality of recessed holes, each hole adapted to accept one of the first plurality of bumps.

10. (currently amended) A semiconductor circuit comprising:

a semiconductor die comprising a first plurality of electrical contacts and a second plurality of electrical contacts;

a first plurality of conductive bumps wherein at least one bump in the first plurality is conductively connected to at least one of the first plurality of electrical contacts;

a second plurality of conductive bumps, wherein at least one bump in the second plurality is conductively connected to at least one of the second plurality of electrical contacts; and

~~wherein each of the bumps in said first plurality of conductive bumps is larger than each of the bumps in said second plurality of conductive bumps.~~

wherein the average size of the first plurality of conductive bumps is at least 20% larger than the average size of the second plurality of conductive bumps.

11. (original) The semiconductor circuit of Claim 10,

wherein the average size of the first plurality of conductive bumps is at least 100% larger than the average size of the second plurality of bumps.

12. (currently amended) The semiconductor circuit of Claim 10,

wherein the average size of the first plurality of conductive bumps is at least 200% larger than the average size of the second plurality of bumps.

13. (canceled)

14. (original) The semiconductor circuit of Claim 10, further comprising:

a built up layer between the die and the second plurality of bumps; and

wherein the first plurality of bumps are substantially coplanar with the second plurality of bumps with respect to their surfaces opposite the surface of the die.

15. (currently amended) A method of making a semiconductor circuit, comprising:  
providing a semiconductor die comprising a first plurality of electrical contacts and a second plurality of electrical contacts;  
conductively connecting to the die a first plurality of conductive bumps wherein at least one bump in the first plurality is conductively connected to at least one of the first plurality of electrical contacts;  
conductively connecting to the die a second plurality of conductive bumps, wherein at least one bump in the second plurality is conductively connected to at least one of the second plurality of electrical contacts; and  
~~wherein each of the bumps in said first plurality of conductive bumps is larger than each of the bumps in said second plurality of conductive bumps.~~  
wherein the average size of the first plurality of conductive bumps is at least 20% larger than the average size of the second plurality of conductive bumps.

16. (canceled)

17. (original) The method of Claim 15, further comprising the step of attaching said semiconductor die to a substrate, wherein at least some of said bumps in said first plurality of bumps fit into holes in said substrate.

18. (original) The method of Claim 15, further comprising:  
forming a built up layer between the die and the second plurality of bumps; and  
wherein the first plurality of bumps are substantially coplanar with the second plurality of bumps relative to the substrate

19. (original) The semiconductor circuit of Claim 15, further comprising:  
forming a built up layer between the substrate and the second plurality of bumps; and  
wherein the first plurality of bumps are substantially coplanar with the second plurality of bumps relative to the semiconductor die.

Appl. No. 10/696,017  
Amtd. dated Dec. 20, 2004  
Reply to Office action of Aug. 26, 2004

20. (original) The semiconductor circuit of Claim 15, further comprising:  
forming a first built up layer between the die and the second plurality of bumps;  
forming a second built up layer between the substrate and the second plurality of  
bumps; and  
wherein the die and substrate are substantially parallel to one another.